Enrollment No: _____ Exam Seat No:_____

C.U.SHAH UNIVERSITY

Summer Examination-2017

Subject Name: Hardware Descriptive Language

Subject Code: 5TE01HDL1 Branch: M.Tech (**VESD)**

Semester: 1 Date: 28/03/2017 Time: 10:30 To 01:30 Marks: 70

Instructions:

(1) Use of Programmable calculator and any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

SECTION – I

Q-1 **Attempt the following questions:** **(07)**

a. What is Verilog HDL?
b. What does UDP stand for?
c. Can a test bench be written using Verilog HDL?
d. What is the key difference between an initial statement and an always statement?
e. Name two logic primitive gates.
f. What do you mean by term module in Verilog HDL?
g. Is there a Boolean type in Verilog HDL?

Q-2 **Attempt all questions** **(14)**

(a) What are the major capabilities of the Verilog hardware description language?
(b) Explain in detail with example behavioral style design in Verilog HDL.

OR

Q-2 **Attempt all questions** **(14)**

(a) Enlist Compiler Directives used in Verilog HDL and explain any four in detail.
(b) Explain in detail with example Mixed style design in Verilog HDL.

Q-3 **Attempt all questions** **(14)**

(a) State different built in primitive gates available in Verilog HDL. Explain any two
(b) Write a model, in behavioral style, for the 8-to-1 Multiplexer.

OR

Q-3 **Attempt all questions** **(14)**

(a) Enlist Data types used in Verilog HDL and explain any four in detail.

(b) Write a model, in structural style, for the 1 bit Full Subtractor.

SECTION – II

Q-4 **Define the following terms** **(07)**

a. What is test bench?
b. When is a label required for a block?
c. Is it necessary to specify a delay in an always statement?
d. What is the difference between a gate instantiation and a module instantiation?
e. How does the casex statement differ from the case statement?
f. Write syntax of Loop Statement.
g. Give an example of how turn-off delay is used in a continuous assignment.

Q-5 **Attempt all questions** **(14)**

(a) Explain in detail MOS switches and Bidirectional switches.
(b) Explain the Edge-triggered Sequential UDP.

OR

Q-5 **Attempt all questions** **(14)**

(a) Explain Net Delays with example in detail.
(b) Explain Initial Assignment statement with example

Q-6 **Attempt all questions** **(14)**

(a) Explain Conditional Assignments statement with example
(b) Explain synthesis in design process.

OR

Q-6 **Attempt all Questions** **(14)**

(a) Explain Case Statement with example
(b) Explain Procedural Assignments statement